

FIG. 1

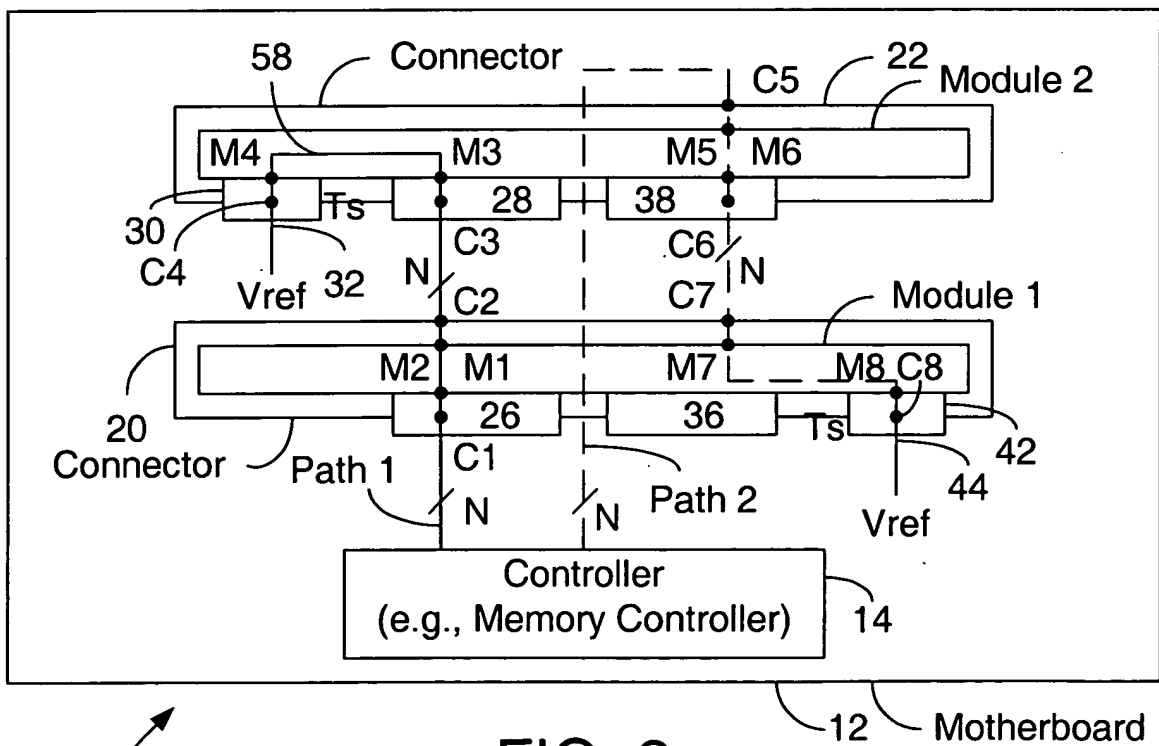


FIG. 2

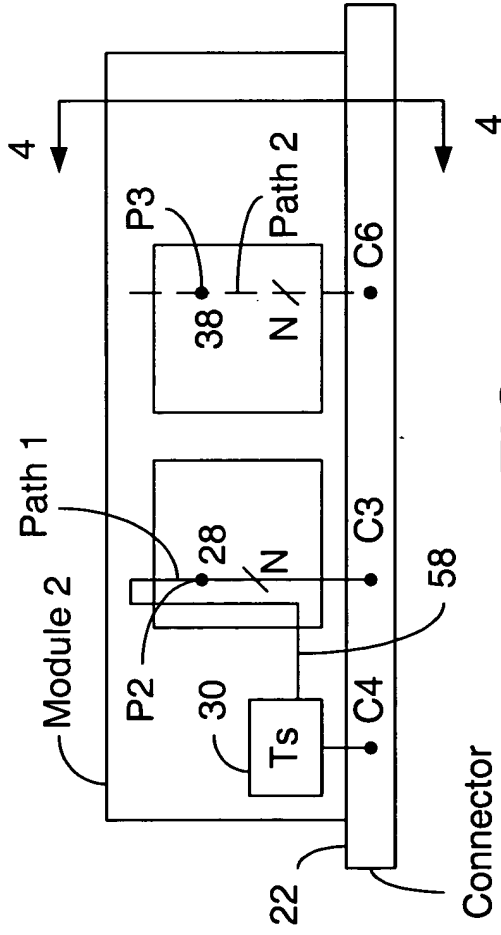


FIG. 3

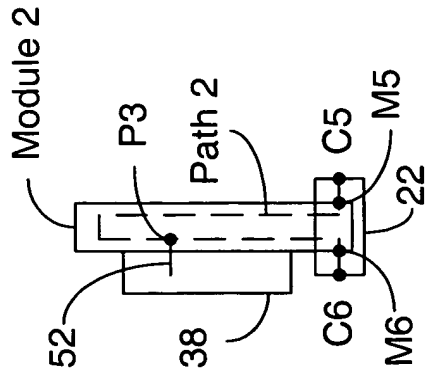


FIG. 4

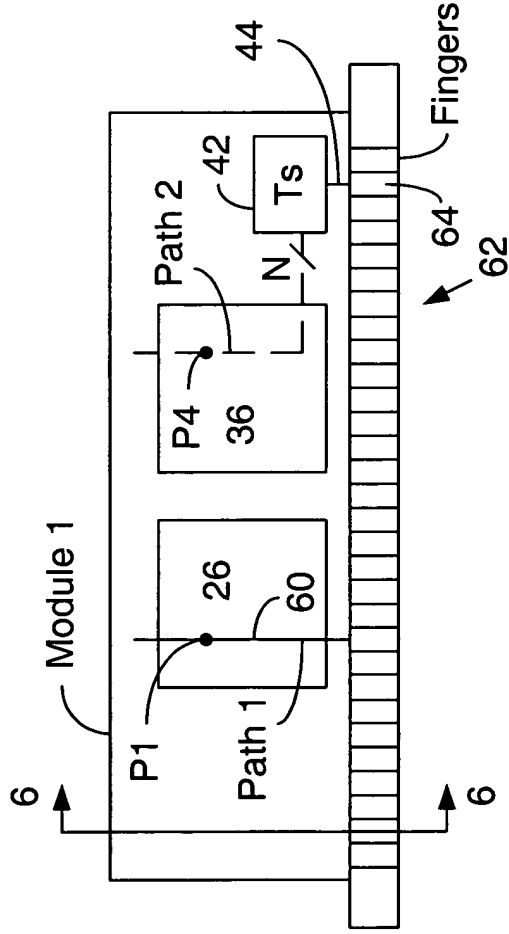


FIG. 5

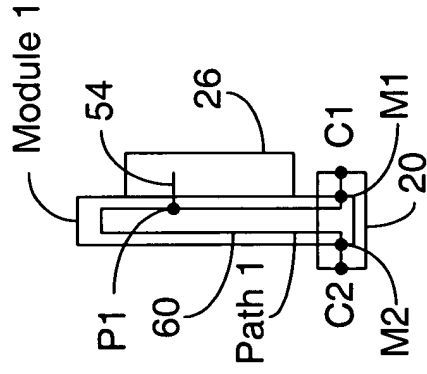


FIG. 6

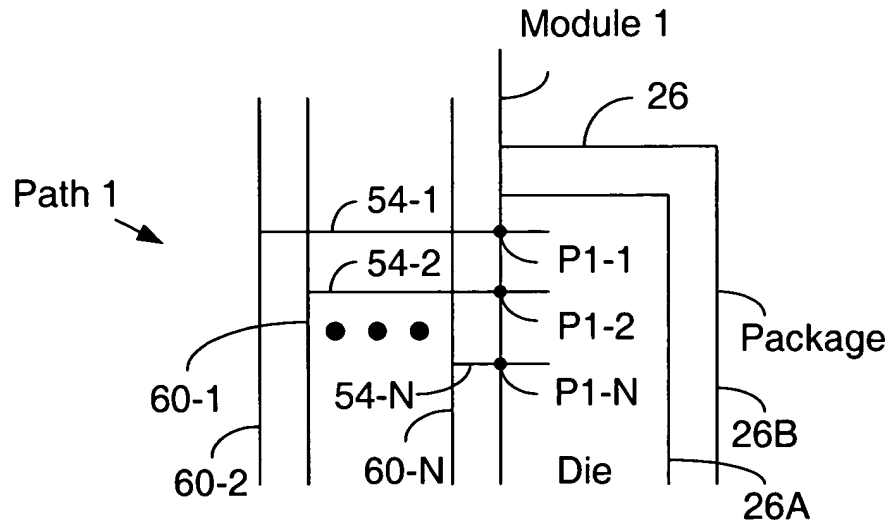


FIG. 7

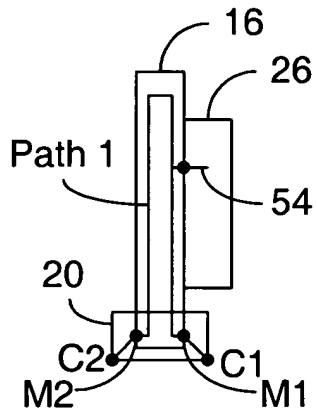


FIG. 8

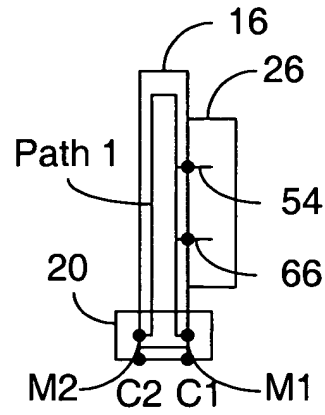


FIG. 9

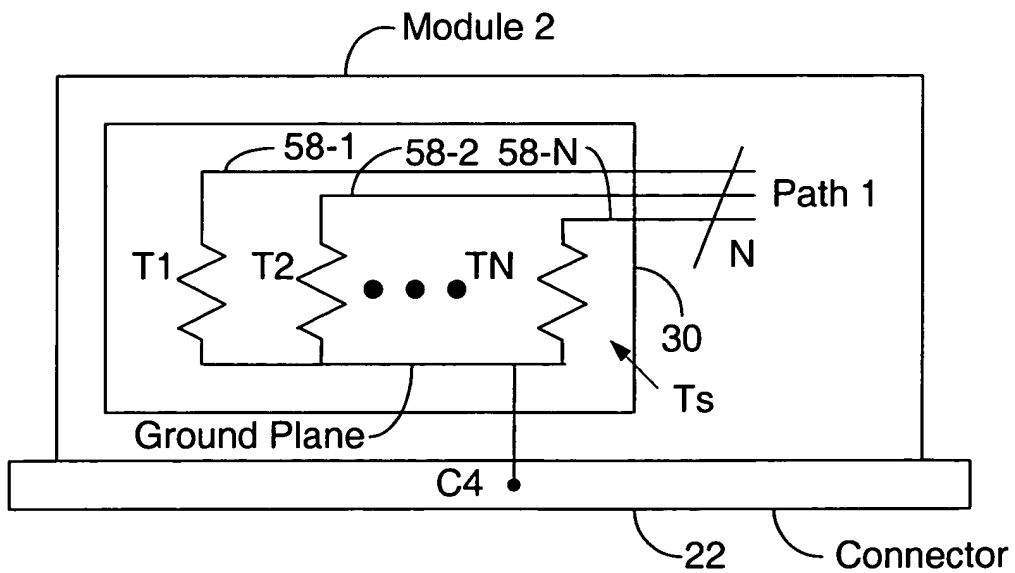
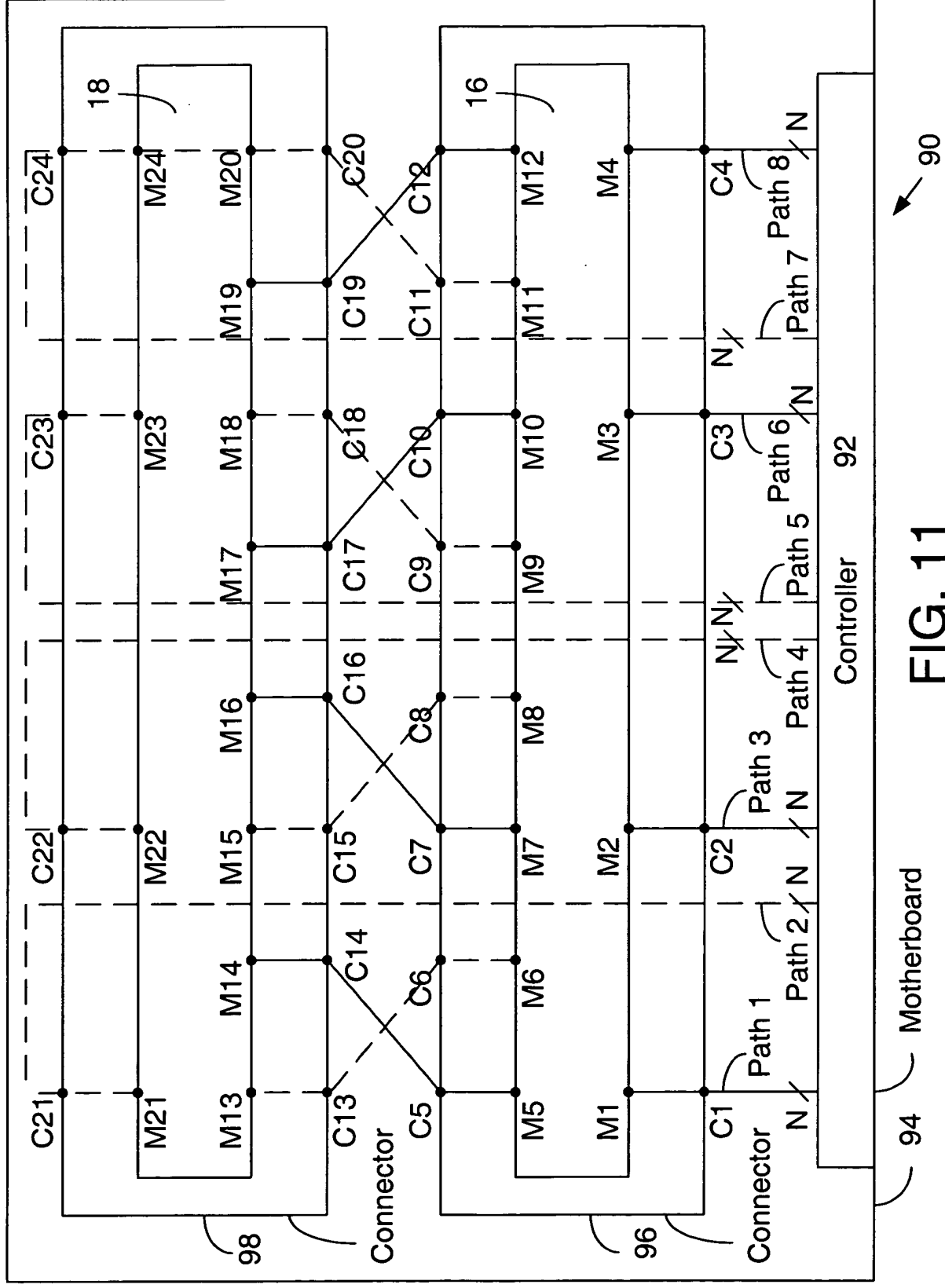
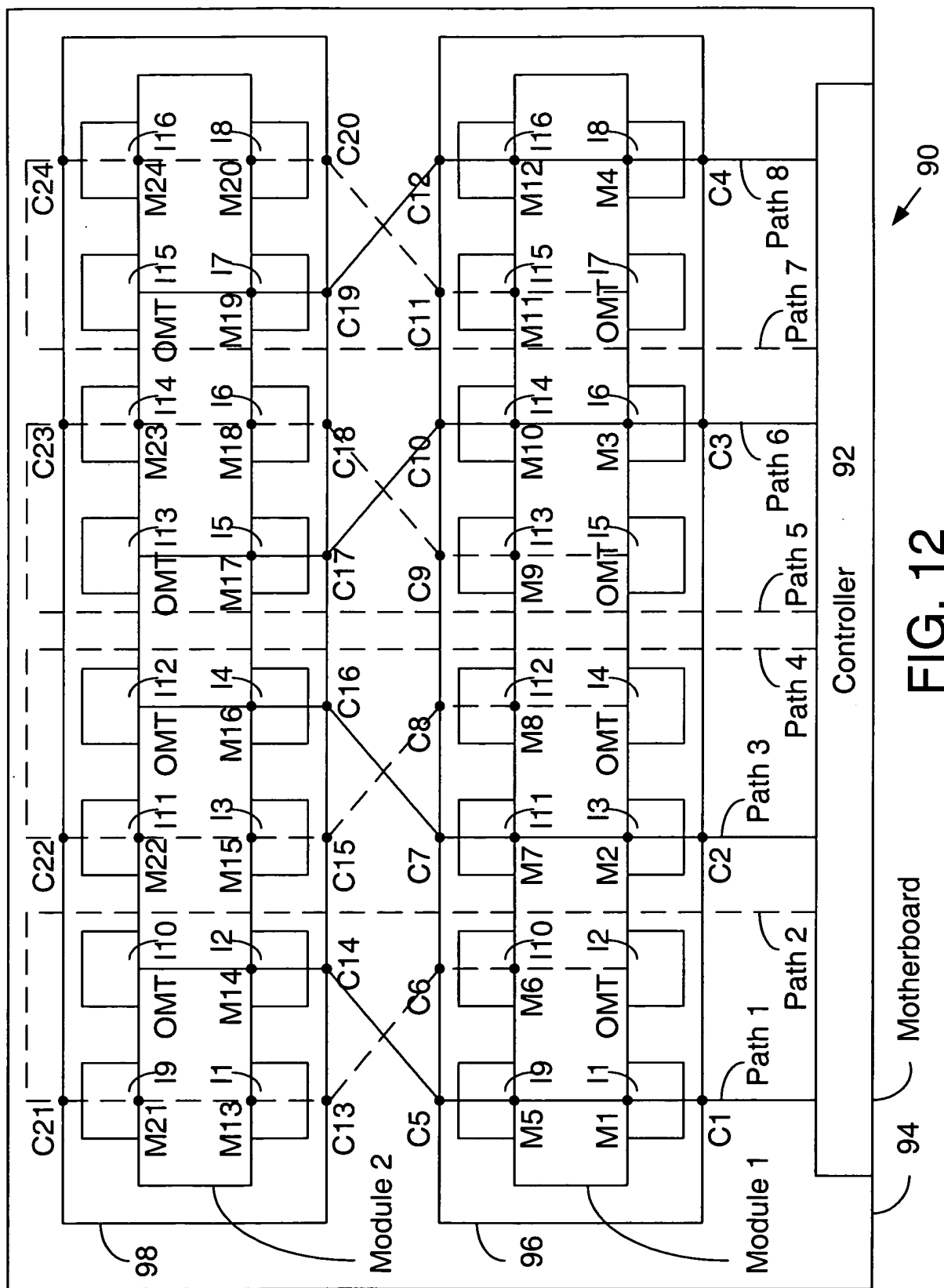
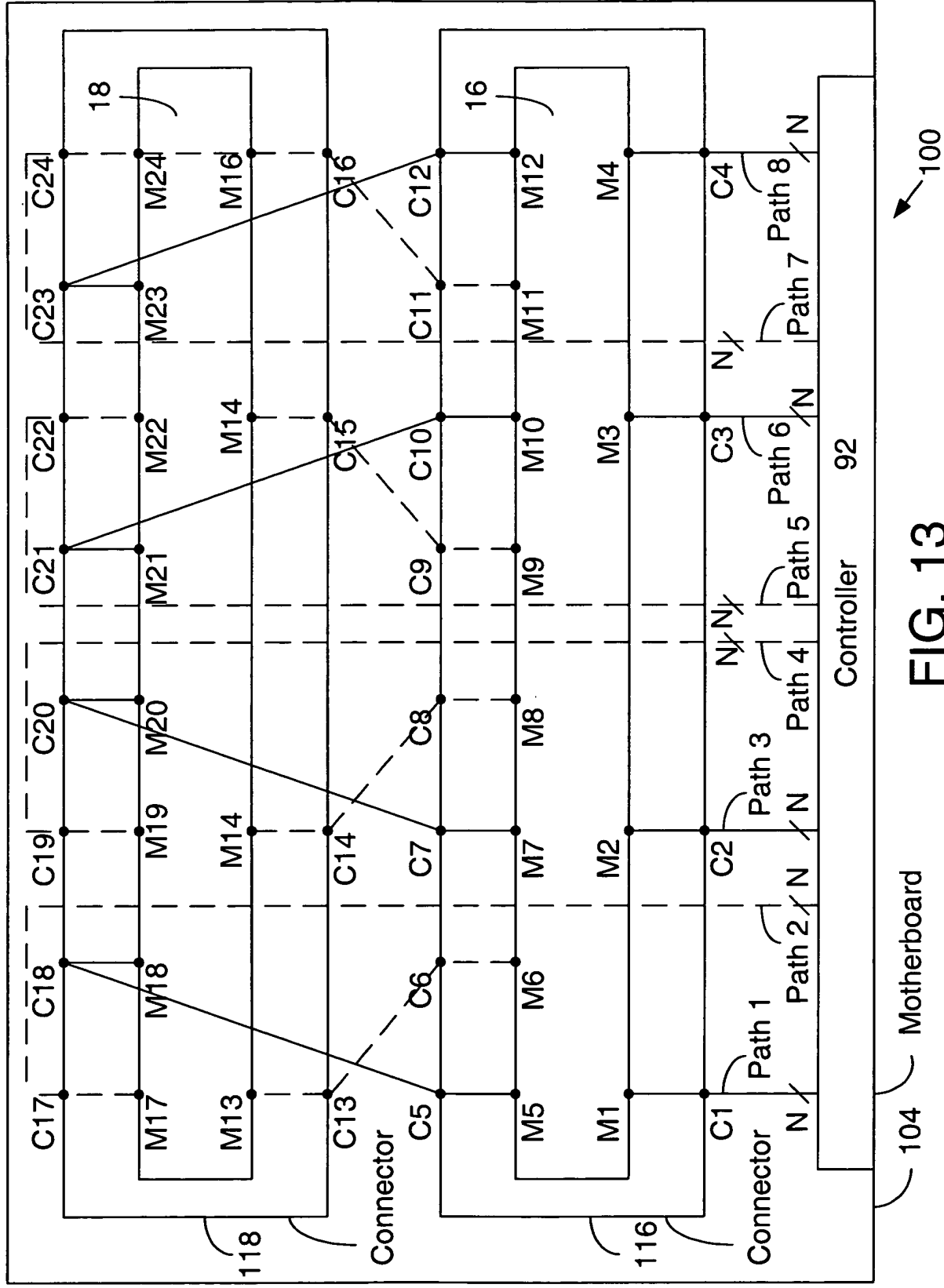


FIG. 10







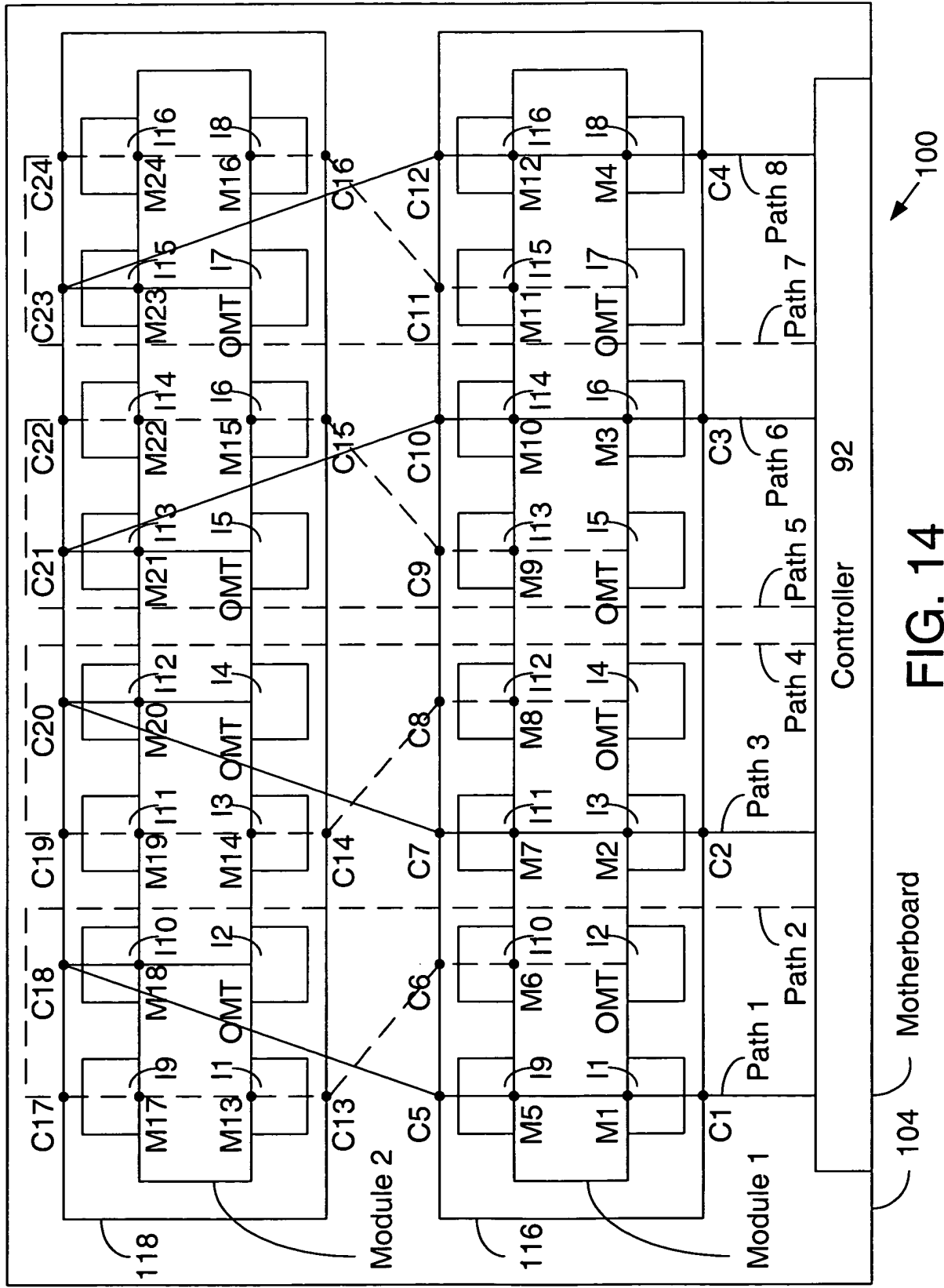


FIG. 14

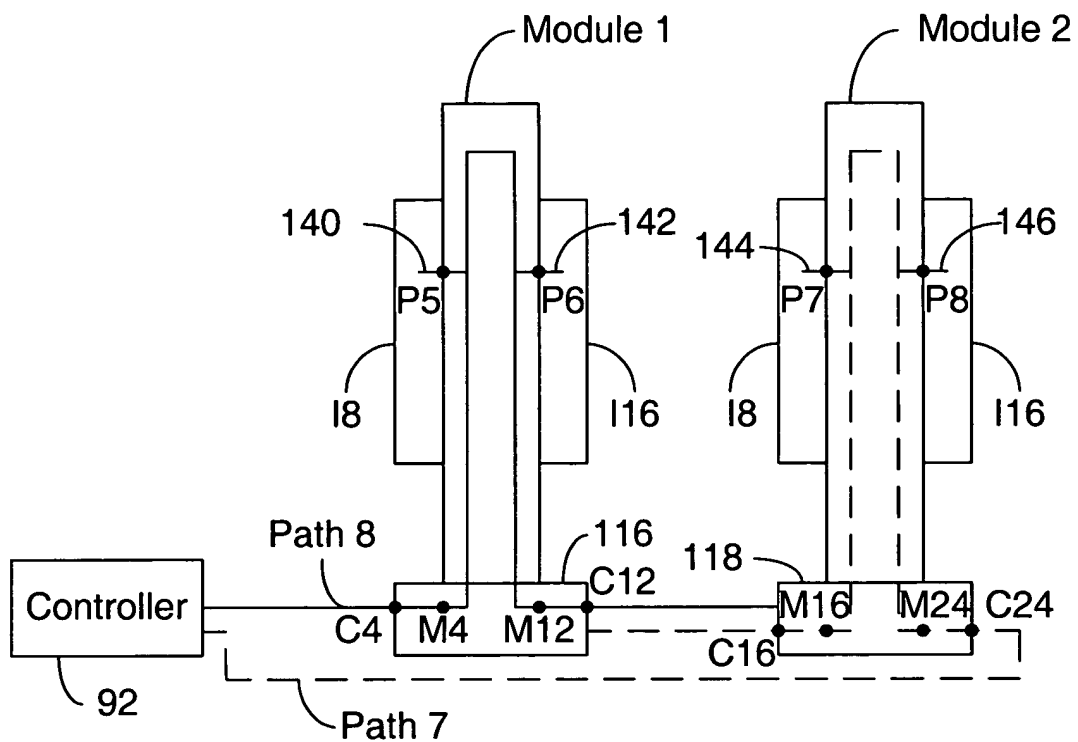


FIG. 15

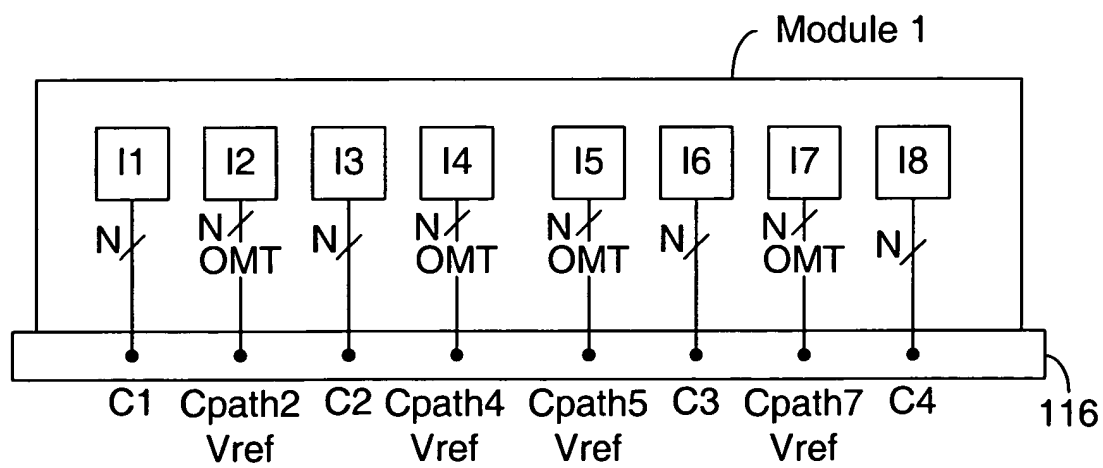


FIG. 16



FIG. 17

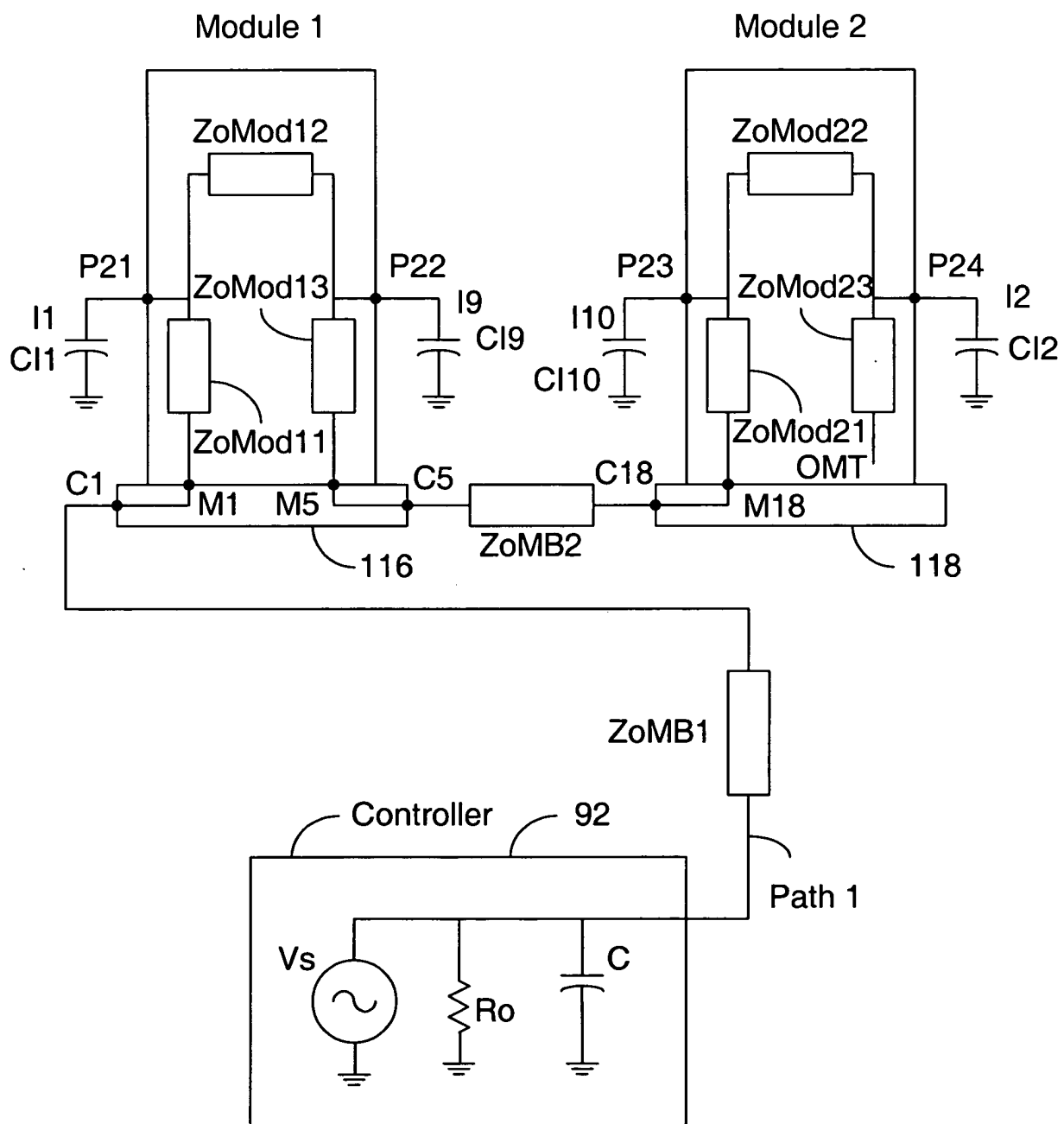


FIG. 17

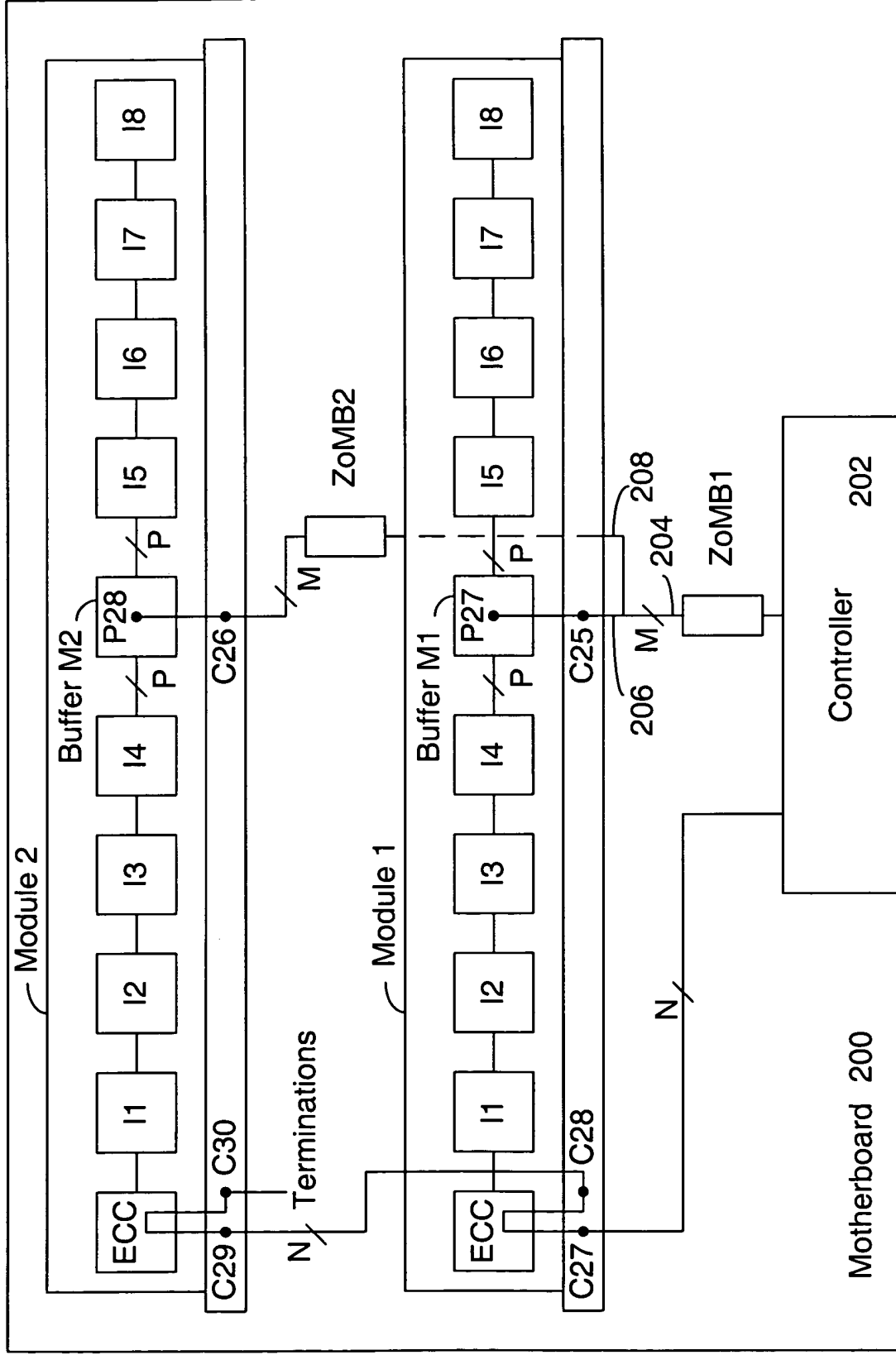


FIG. 18

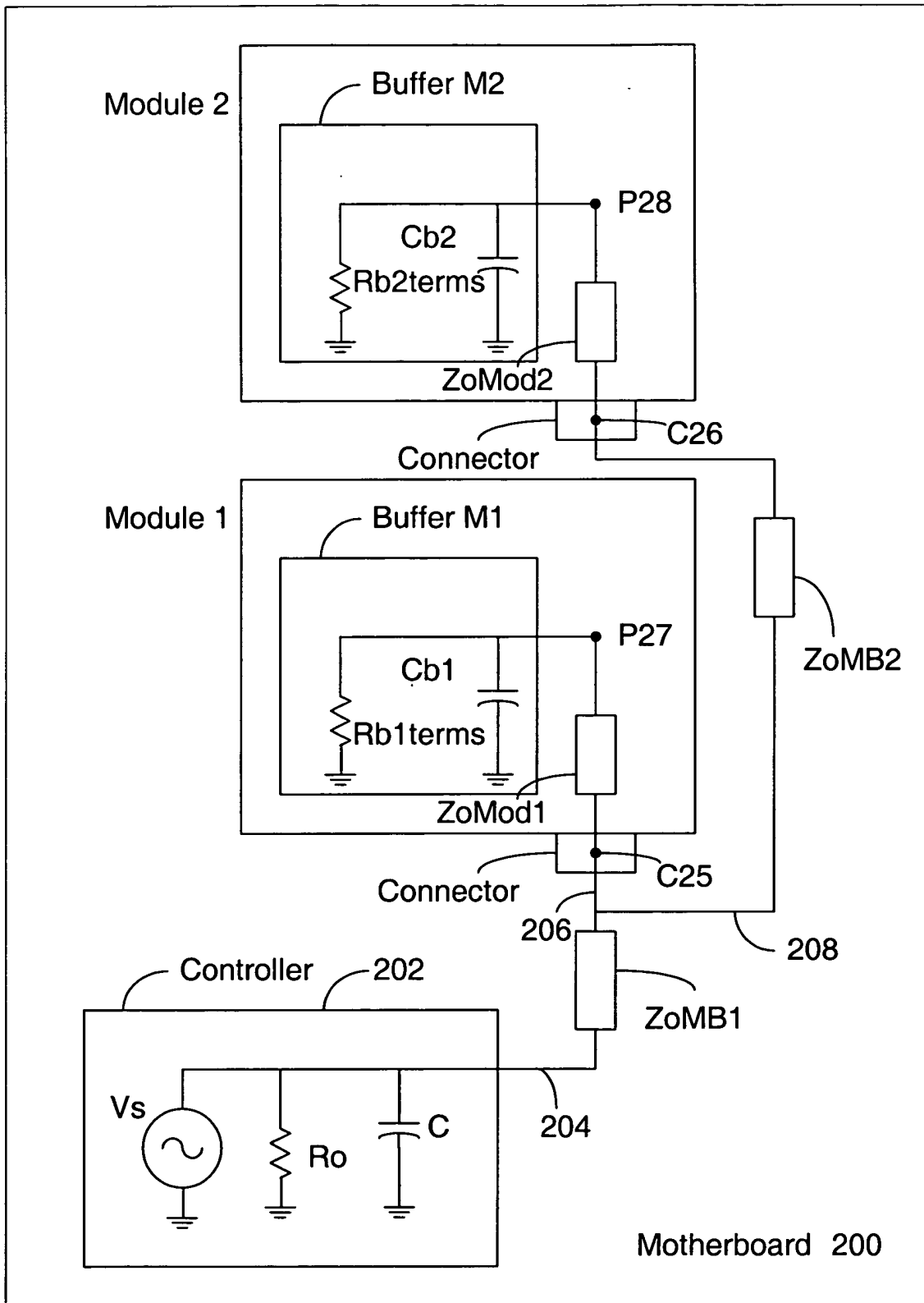


FIG. 19

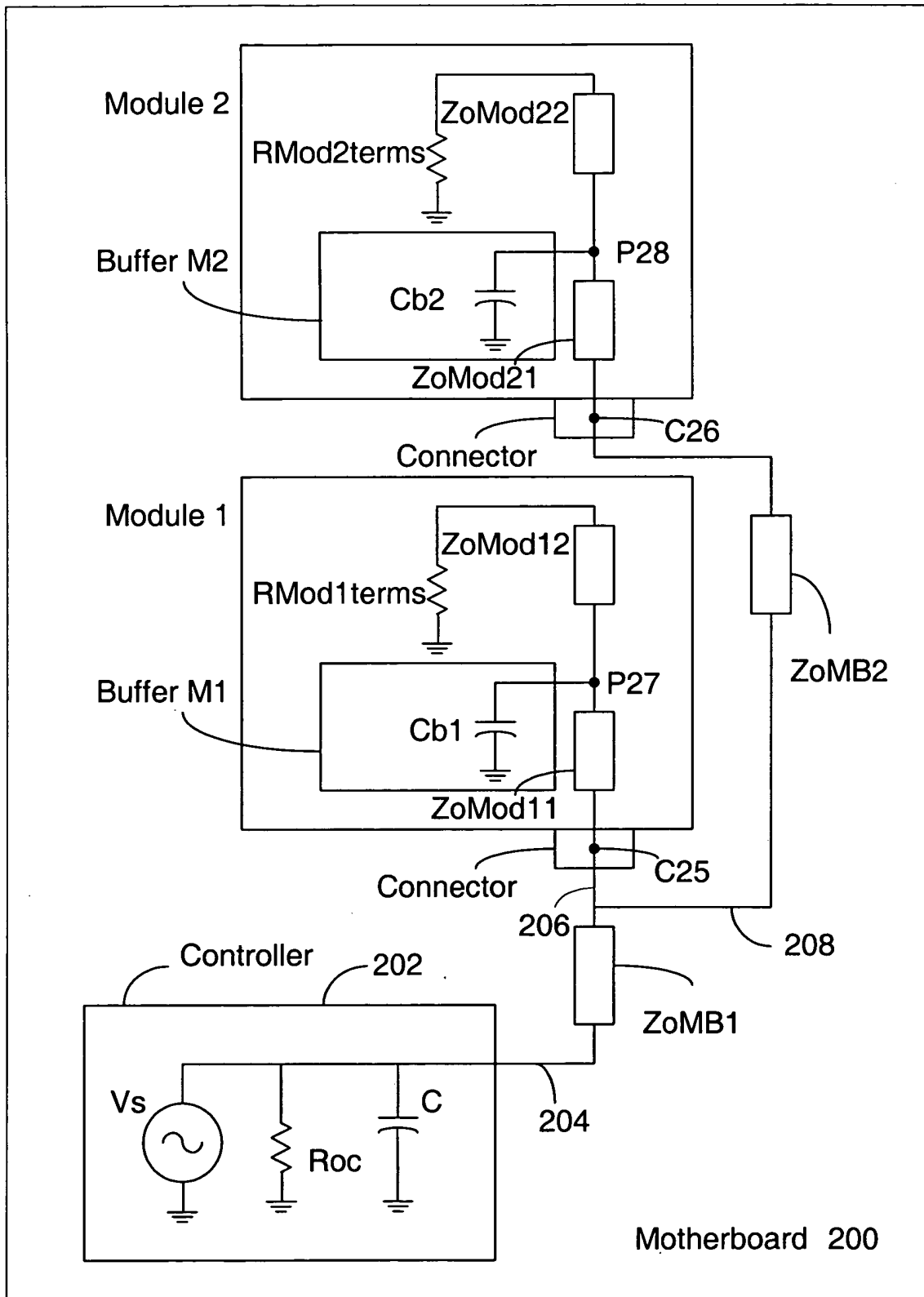


FIG. 20

The diagram illustrates a system architecture with two main modules, Module 1 and Module 2, and a central Controller. Module 1 is divided into two sub-modules, I1 and I2, which are further divided into I9 and I10. Module 2 is similarly divided into I1 and I2, which are further divided into I9 and I10. The Controller provides a Clk signal to Module 1 and a Terms signal to Module 2. Data paths are labeled Path 1 and Path 2. Various control signals (C1, C5, C6, C60, C61, C17, C13, C62, C63, C18) are shown connecting the modules and the controller.

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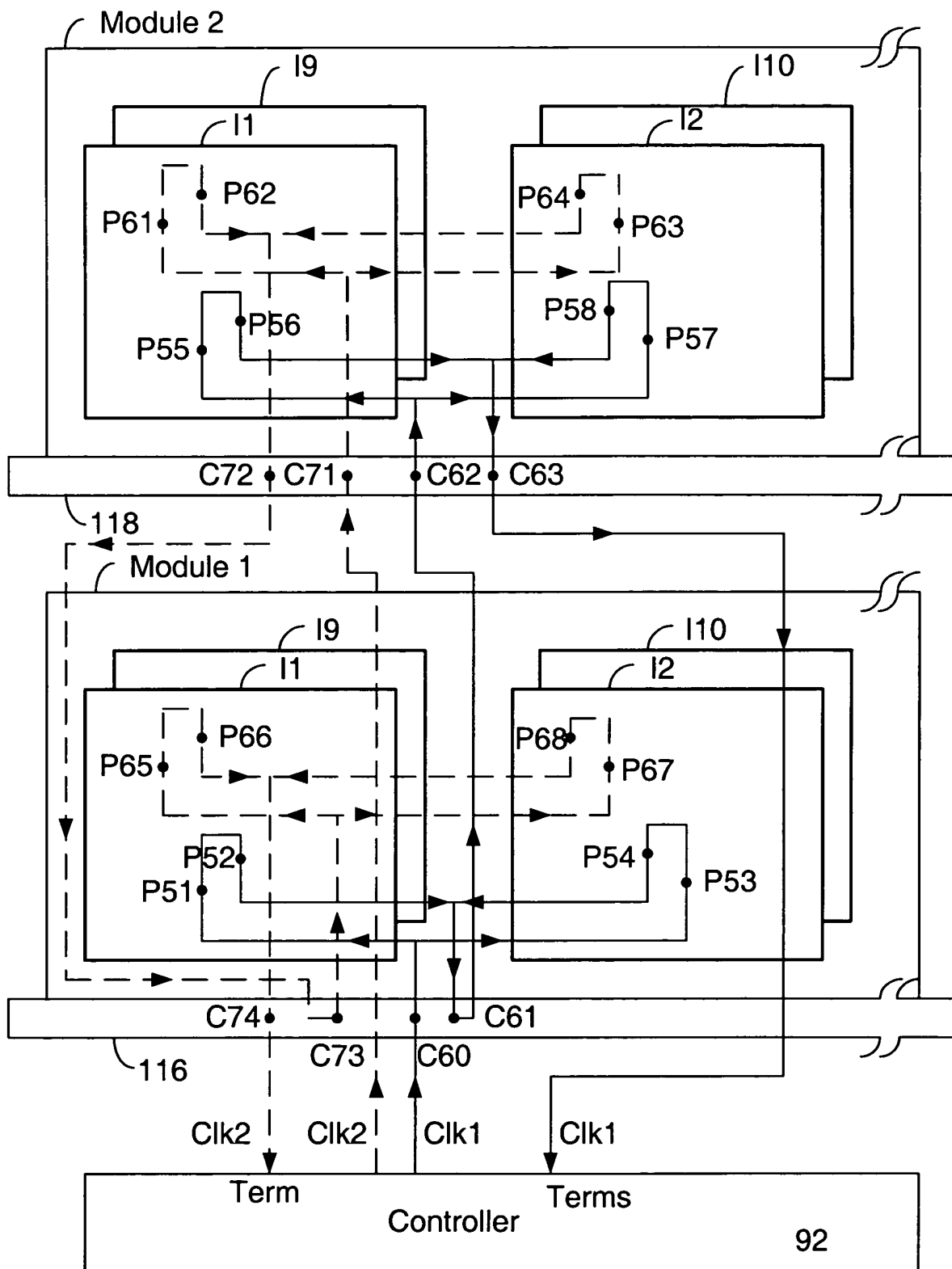
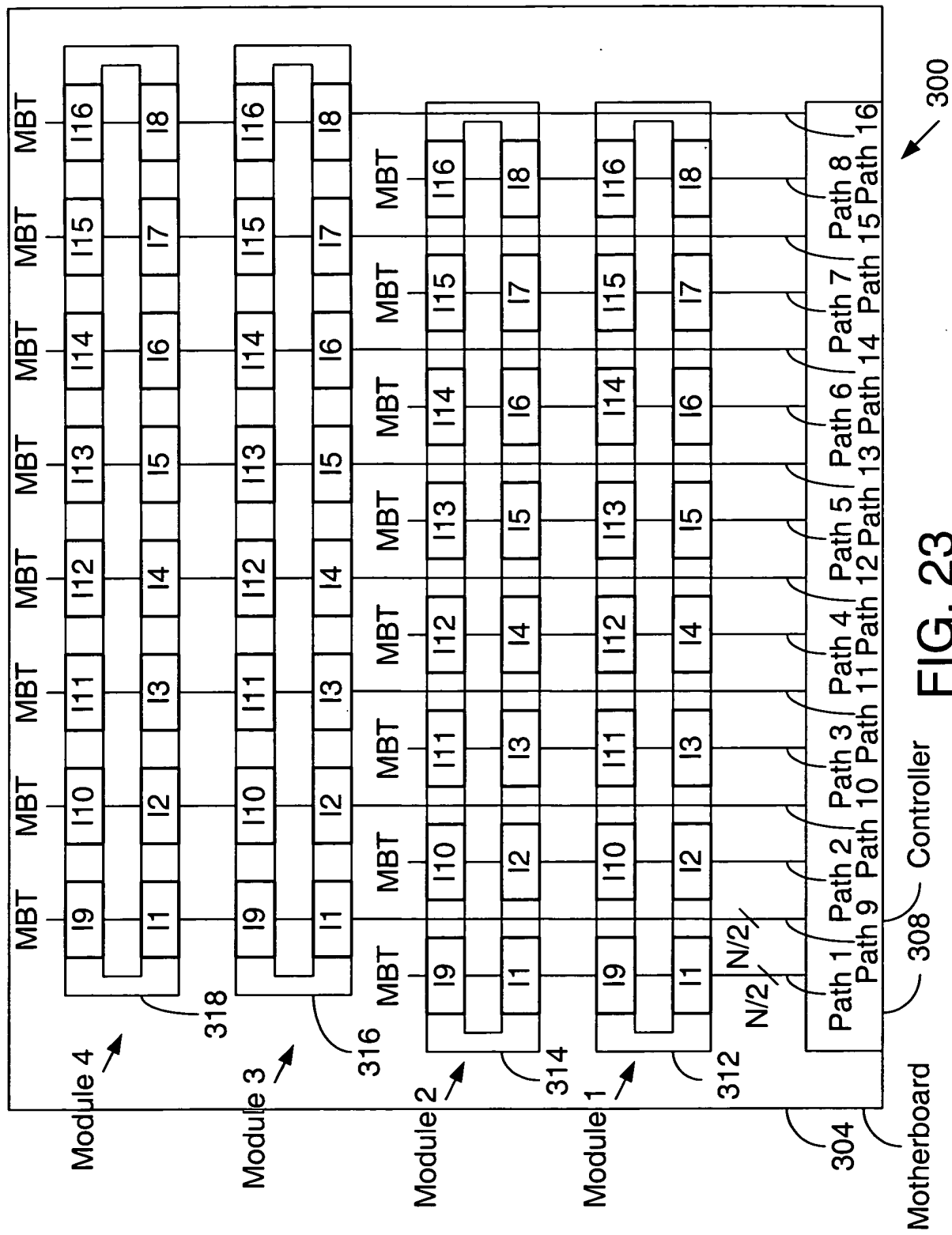


FIG. 22



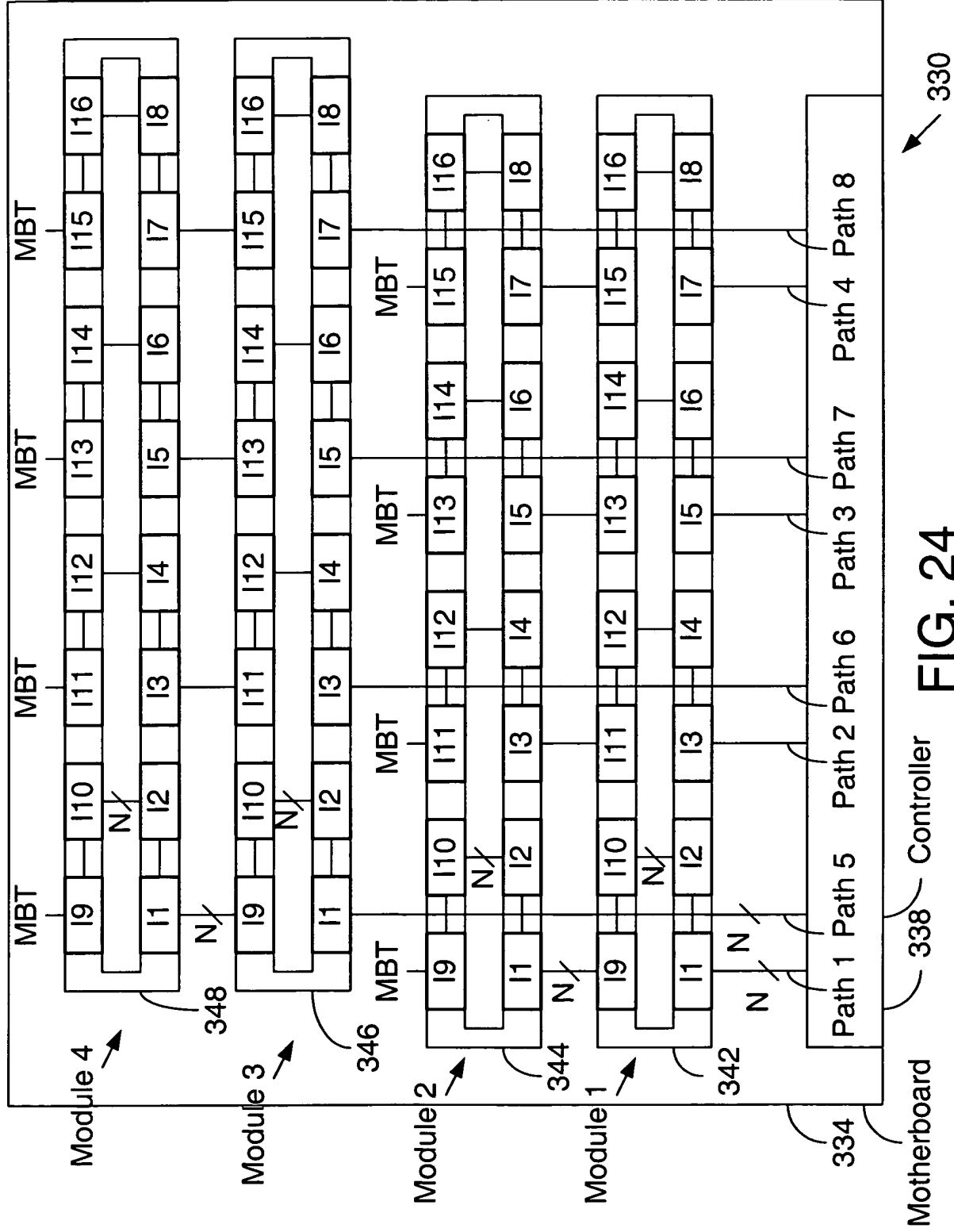


FIG. 24



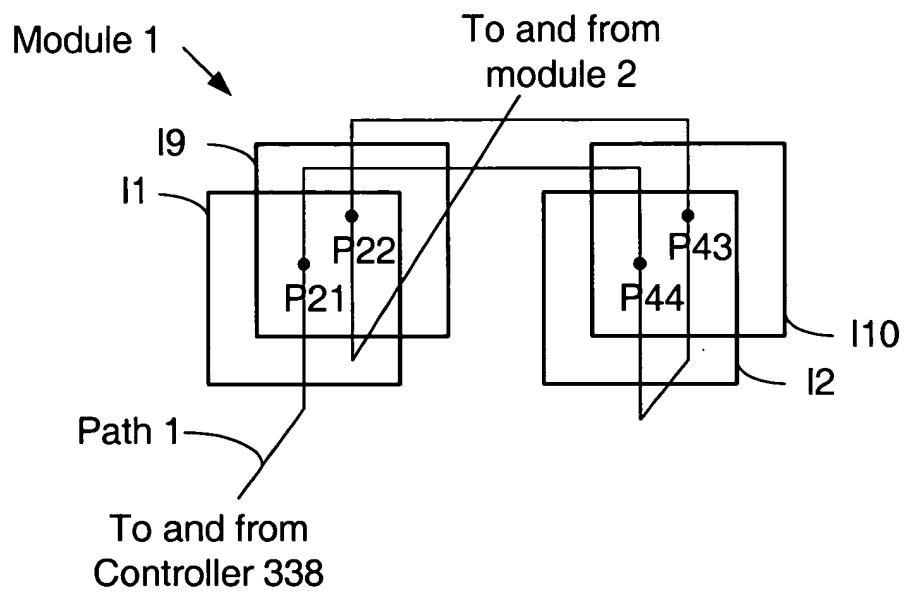


FIG. 25

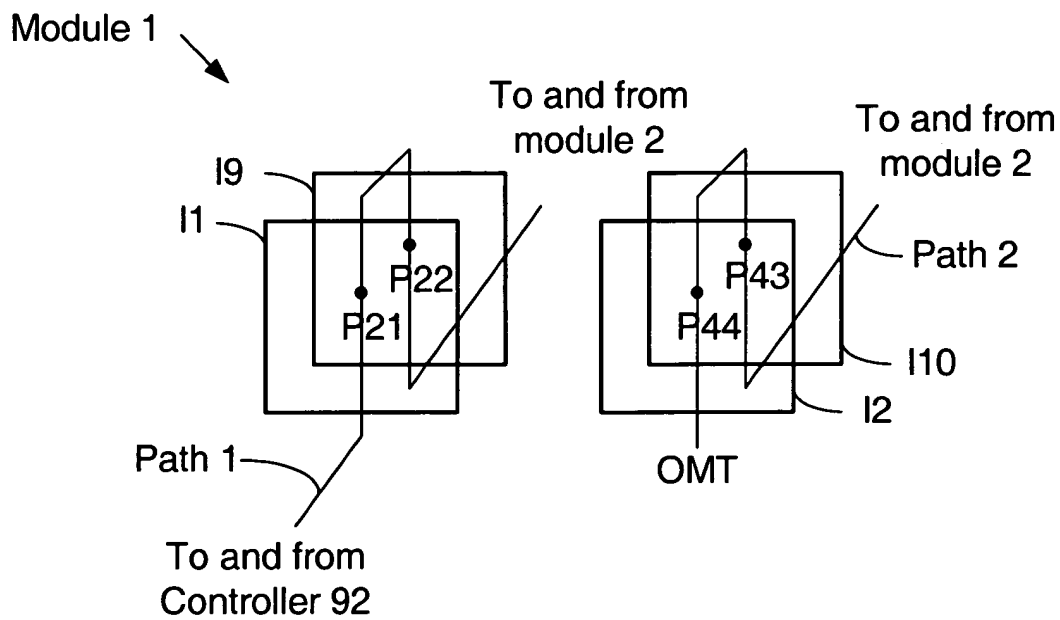


FIG. 26

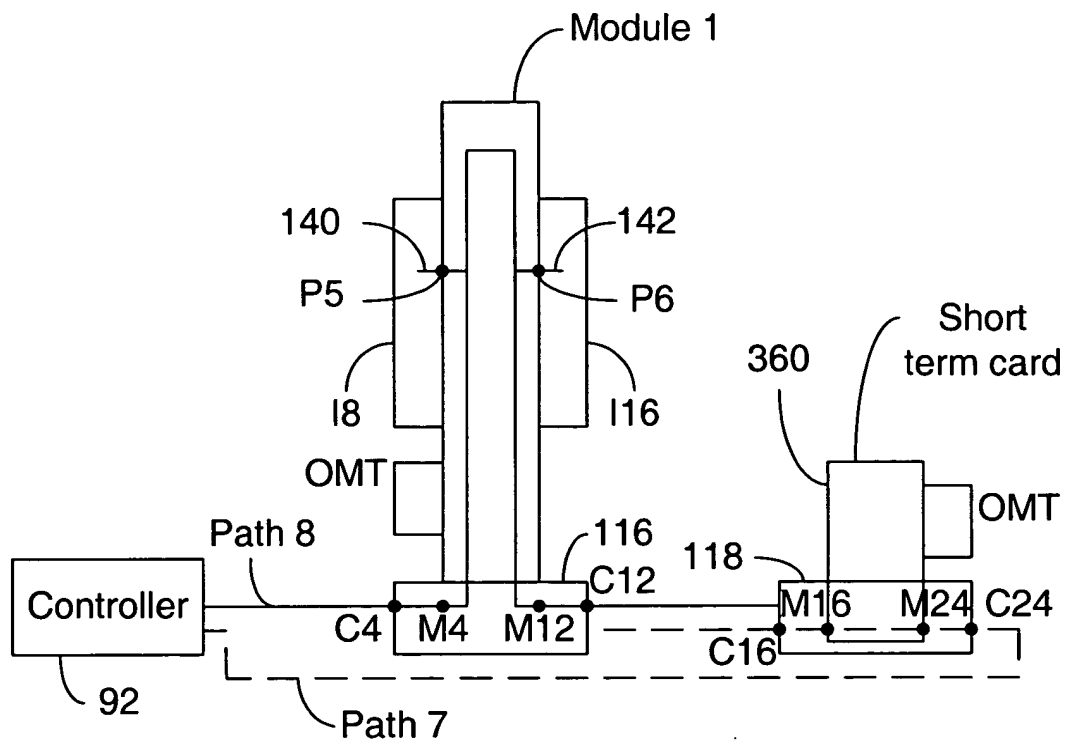


FIG. 27

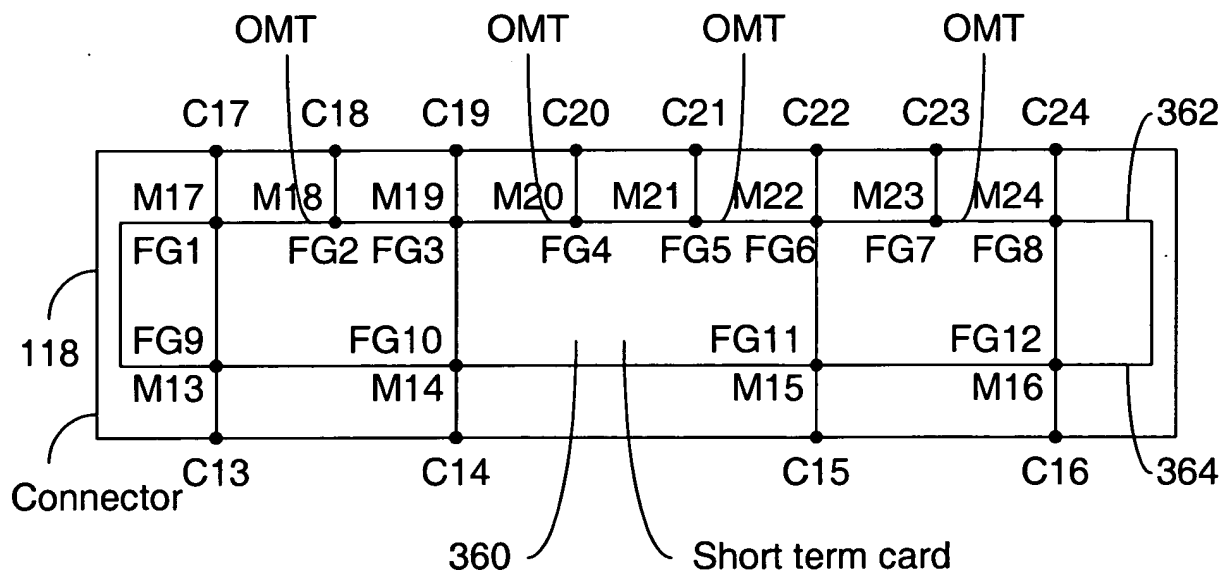


FIG. 28

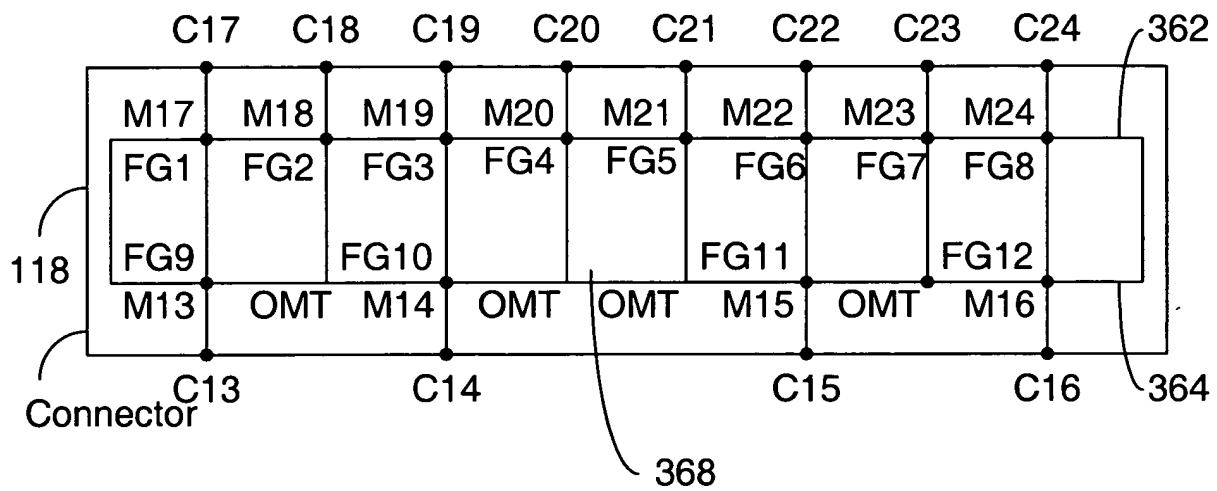


FIG. 29

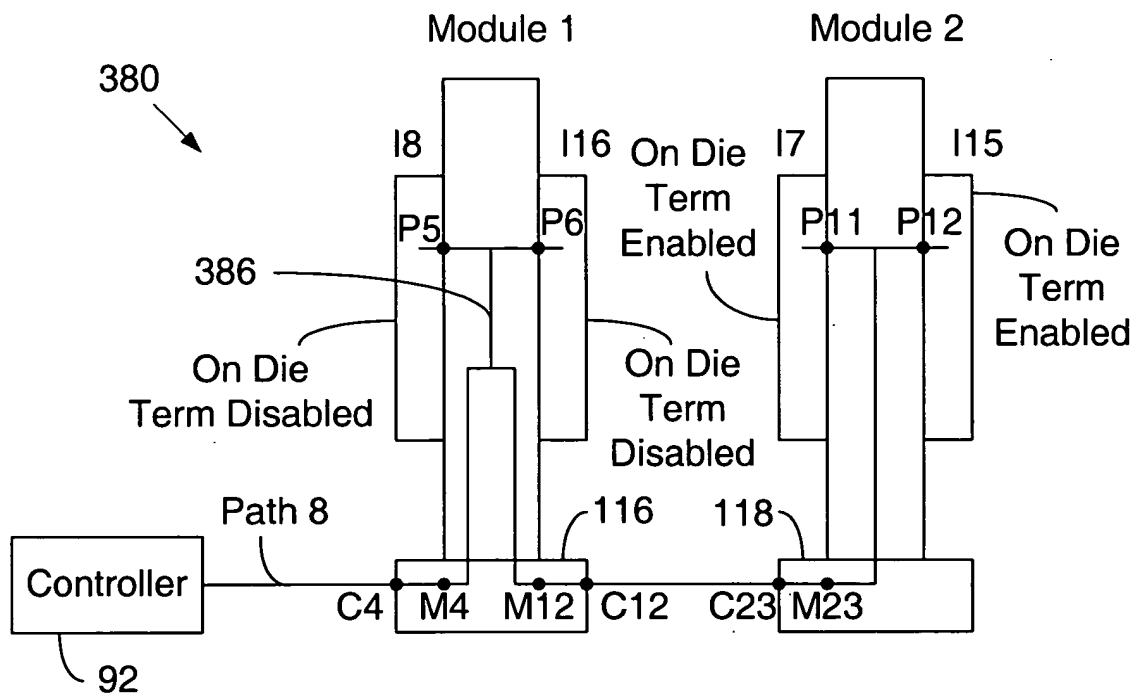


FIG. 30

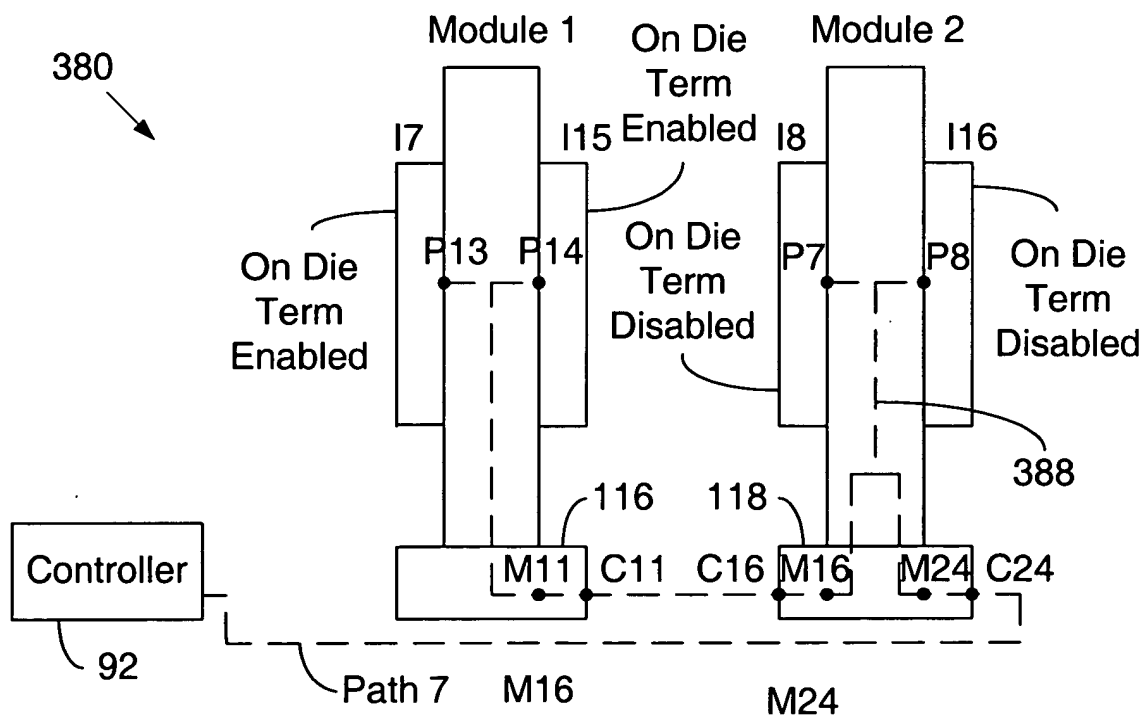


FIG. 31



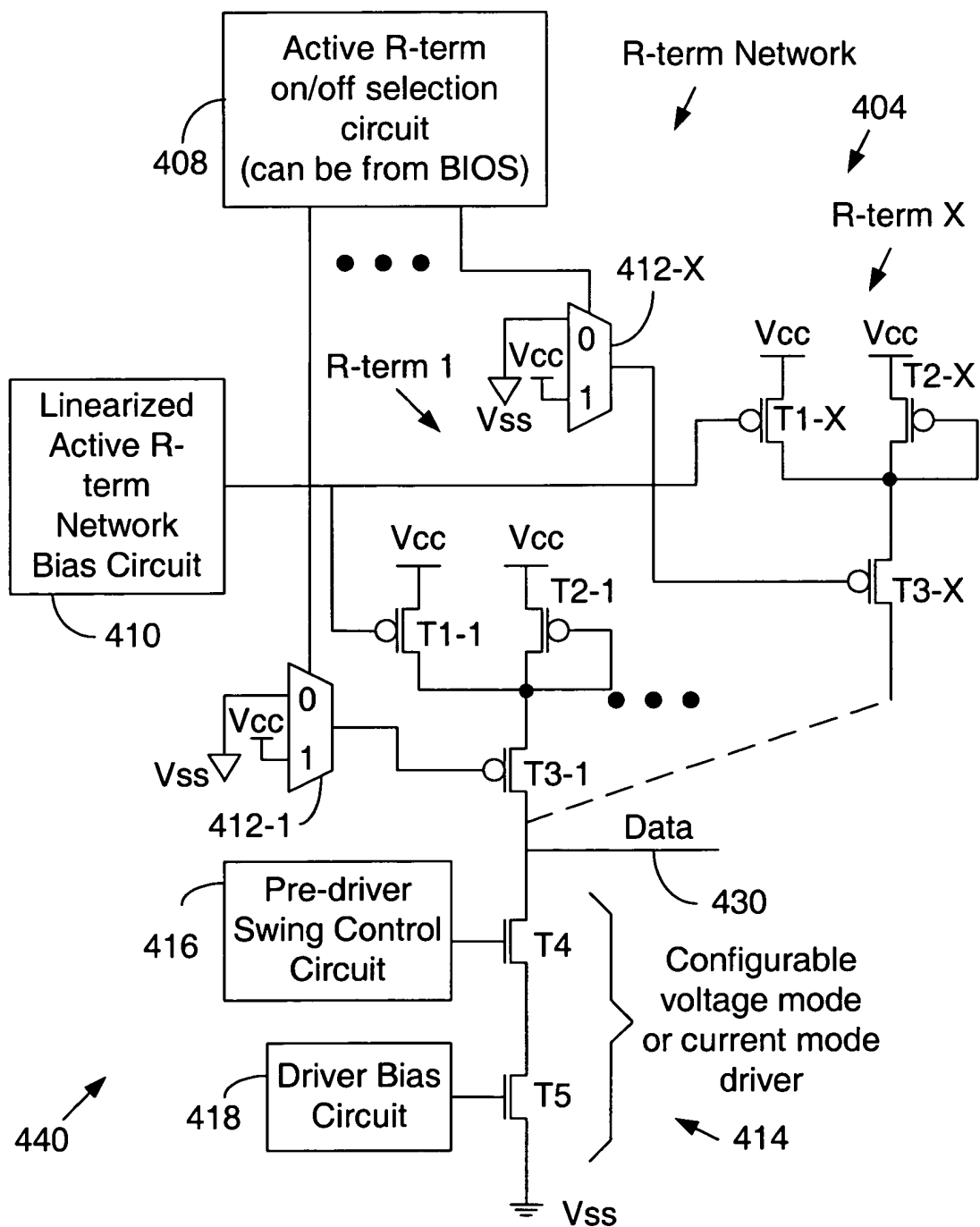
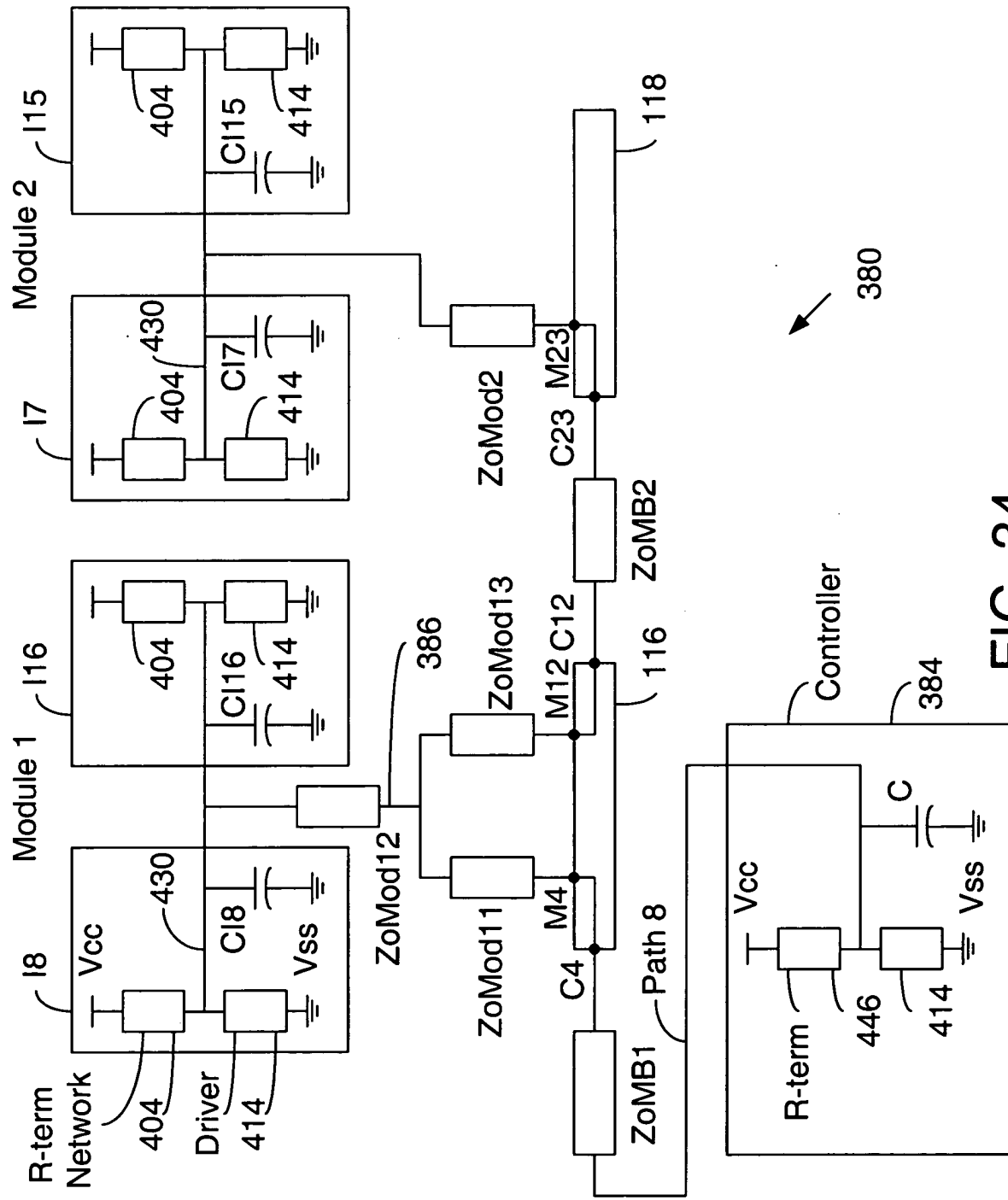
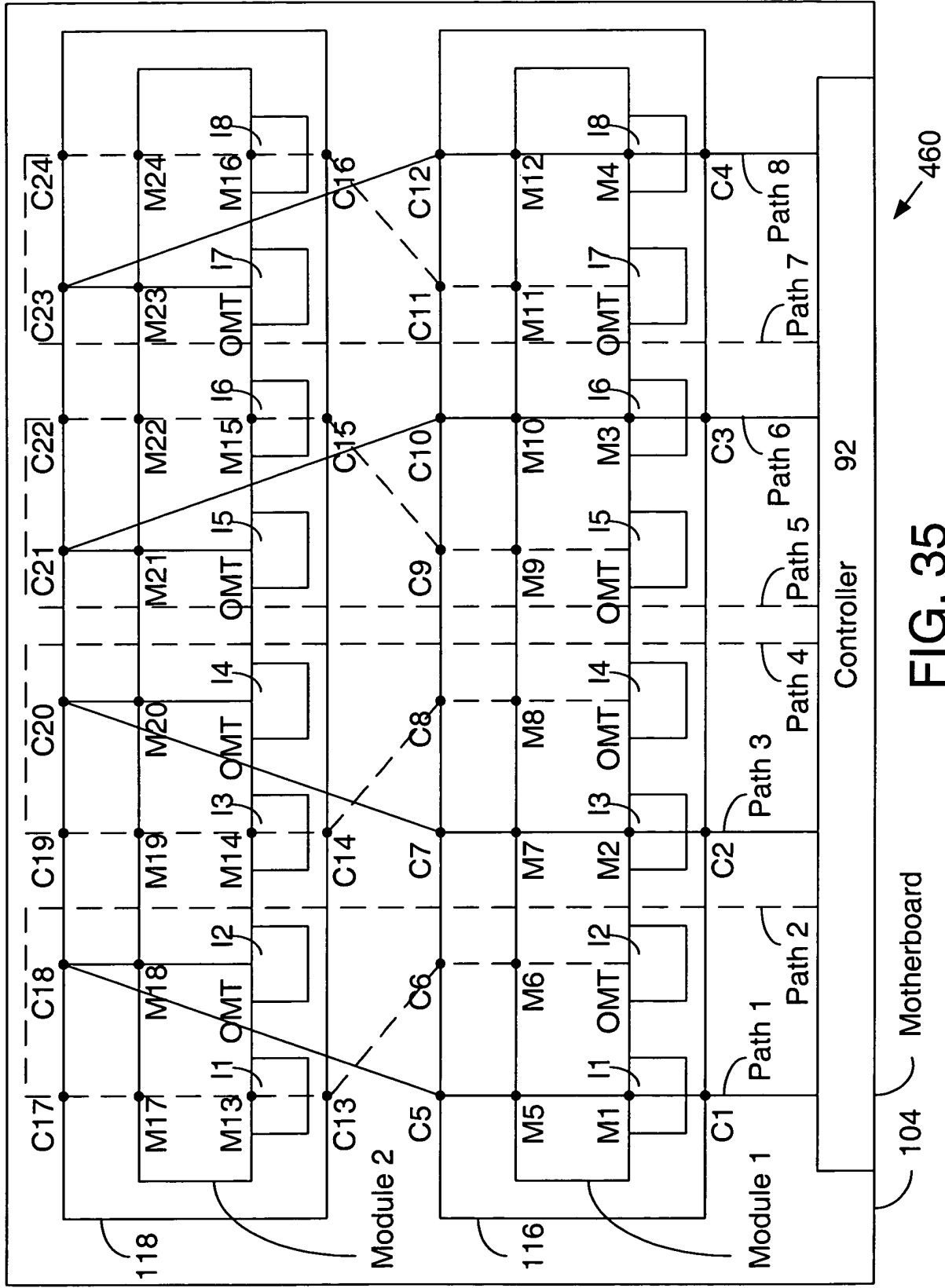


FIG. 33







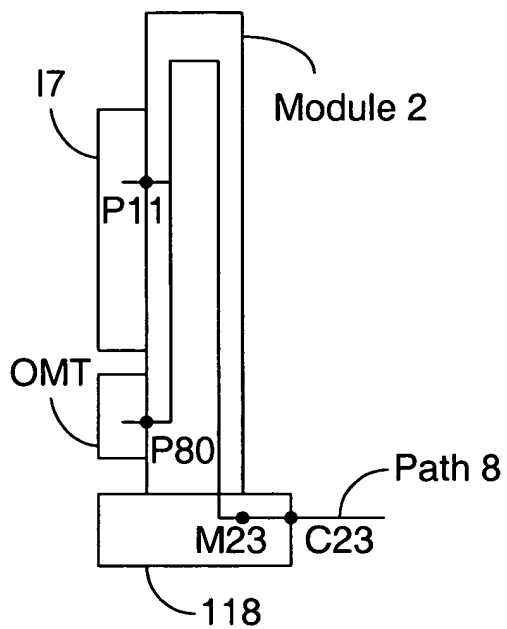


FIG. 36

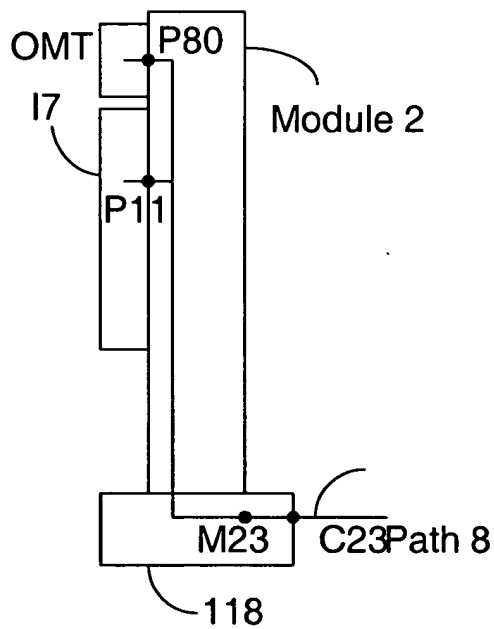


FIG. 37

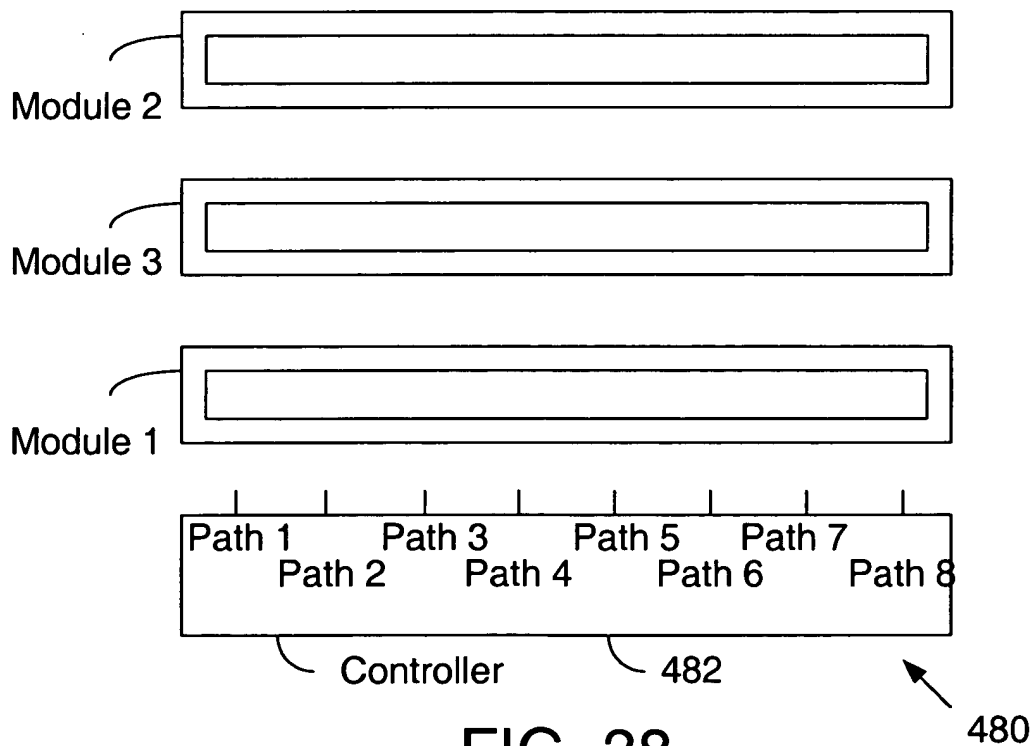


FIG. 38

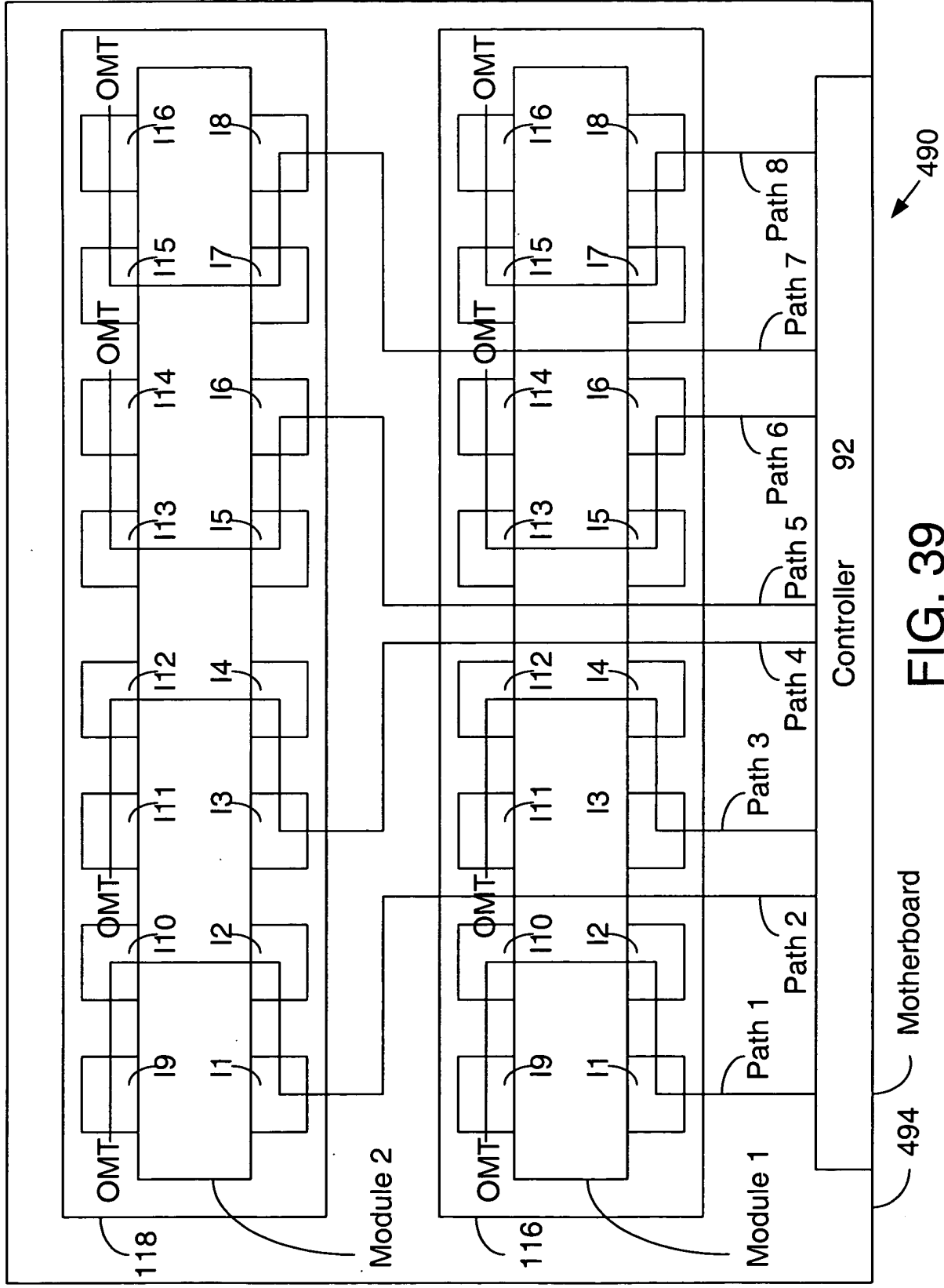


FIG. 39